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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| EXAMINER | |
|---|---|
| CAO, DIEM K | |
| **ART UNIT** | **PAPER NUMBER** |
| 2194 | |

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/348,783 | MA ET AL. | |
| | Examiner | Art Unit | |
| | Diem K Cao | 2126 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.



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## DETAILED ACTION

1. Claims 1-19 are pending. Applicant has amended claims 1 and 13.

### *Continued Examination Under 37 CFR 1.114*

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/29/2004 has been entered.

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-5 and 7-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robinson (U.S. 5,708,838, now refer as Robinson-1) in view of Robinson (U.S. 6,567,837 B1, now refer as Robinson-2).

5. **As to claim 1**, Robinson-1 teaches a host processor (host processor; col. 13, lines 1-8) including a host communication infrastructure configured to provide communication with the

host processor (the comms and interface routines; col. 12, line 66- col. 13, line 8), a plurality of class processors (a plurality of object oriented processors 104, 106, 108), and a plurality of application program interface modules each configured to provide an interface between the host communication infrastructure and at least one class processor (Each of the object oriented processors includes a Comms interface ... to the host processor 102; col. 7, lines 35-60), the application program interface modules each defining a programming interface for a respective class processor (Each of the object oriented processors ...conventional manner; col. 7, lines41-49 and The comms and interface routines ... processor (the library expose the interface to be called while the implementation inaccessible from uses); col. 13, lines 3-6 and the functionality of the pins ... the user interface 104; col. 14, lines 10-14), wherein each class processor responds to selected data messages on the HCI to perform selected computations (each object oriented processor according to the invention is designed with a specific functionality; col. 14, lines 1-14 and the intelligent message handler ... serviced by it, when the host communicates ... each object oriented processor only responses to messages appropriate to it; col. 8, lines 1-35).

6. However, Robinson-1 does not teach a plurality of class processors each having an associated private localized read/write memory, and each class processor responds to selected data messages on the HCI to perform selected computations utilizing the read/write memory. Robinson-2 teaches a plurality of class processors each having an associated private localized read/write memory (col. 17, line 56 – col. 18, line 2 and One or more other parts of RAM are ... its functionality; col. 10, lines 11-41), and each class processor responds to selected data messages to perform selected computations utilizing the read/write memory (One or more other

parts of RAM are ... its functionality; col. 10, lines 11-41 and the input message ... for named instantiation of the object; col. 5, lines 44-52).

7. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Robinson-1 and Robinson-2 because it provides an object oriented processor array that utilizes memory in an efficient manner (col. 4, lines 23-25).

**8.** **As to claim 2**, Robinson-1 does not teach the distributed processing system is integrated onto a single chip substrate. Robinson-2 teaches the distributed processing system is integrated onto a single chip substrate (resides on a single chip; col. 7, lines 59-61).

9. **As to claim 3**, Robinson-1 teaches each of the plurality of class processors is configured to perform operations on a selected proper subset of application objects (each object oriented processor according to the invention is designed with a specific functionality; col. 14, lines 1-14 and the code for the object oriented processors and the host ... be written as the main; col. 17, lines 62-67).

10. **As to claim 4**, Robinson-1 teaches the processors are configured to reference other class processors, if at all, only through their respective application program interface modules (allow for direct ... generate messages within the object oriented processor; col. 18, lines 1-30), without reference to data structures operated upon by other referenced class processors (and the code for the object oriented processors and the host ... be written as the main; col. 17, lines 62-67).

11. **As to claim 5**, Robinson-1 teaches the plurality of class processors comprise a plurality of classes of class processors (two or more object oriented processors having the same type of task; col. 8, lines 35-38). However, Robinson-1 does not teach at least one of the class processors has an associated protected localized read/write memory accessible only to itself and to at least one other class processor of the same class. Robinson-2 teaches at least one of the class processors has an associated protected localized read/write memory accessible only to itself and to at least one other class processor of the same class (When an object is instantiated ... their allocated RAM in this manner; col. 10, lines 30-35 and the microprocessors 523a-c provide separate processors for each instantiation of an object ... loading software into one of the processors 523a-c; col. 17, line 63 - col. 18, line 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Robinson-1 and Robinson-2 because it provides an object oriented processor array with enhanced post-manufacture configurability.

12. **As to claim 7**, Robinson-1 teaches the plurality of class processors each further comprise a special purpose processor (floating point processor; col. 6, lines 45-59). However, Robinson-1 does not teaches a special purpose processor coupled to the private localized read/write memory, and public read/write memory, and the public read/write memory is configured to be addressable both to the host processor via the HCI and to the special purpose processor. Since the special purpose processor is used to carry out certain functionality in the class processor, it would have been obvious it has to have access to both private localized read/write memory (in the same

processor) and public memory.

13. **As to claim 8**, Robinson-1 teaches the plurality of class processors comprise a plurality of classes of class processors (the first object oriented processor 104, the second processor 106, the third processor 108; col. 7, line 62 – col. 8, line 27 and there are two or more object oriented processors having the same type of task; col. 8, lines 35-38 and the code for each object oriented processor would be written as a class; col. 17, lines 62-67), and the distributed processing system is configured to restrict direct data communication between the class processors to data communication between class processors of the same class (generates messages within the object oriented processor ... from the host processor; col. 18, lines 1-30 and the object oriented processors communicate with the host processor and with each other via the "comms link" or "comms bus"; col. 20, lines 34-39).

14. **As to claim 9**, Robinson-1 does not teach at least a first class processor and a second class processor of the same class, the first class processor further comprises a protected localized read/write memory, and the first and second class processor are configured so that the protected localized read/write memory of the first class processor is addressable by the second class processor. Robinson-2 teaches at least a first class processor and a second class processor of the same class (active object 23a, 23b; col. 8, lines 9-12 and an object is instantiated by loading software into one of the processors 523a, etc; col. 18, lines 1-2), the first class processor further comprises a protected localized read/write memory (the first part is ... the source ID; col. 10, lines 30-34), and the first and second class processor are configured so that the protected

localized read/write memory of the first class processor is addressable by the second class processor (This first part is common to all object ... one or more other parts of RAM are arranged for private data used by the instantiated object; col. 10, lines 34-41). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Robinson-1 and Robinson-2 because it provides a method to utilize memory in an efficient manner.

15. **As to claim 10**, Robinson-1 does not teach at least one class processor further comprises a public localized read/write memory and the class processor having the public localized read/write memory is configured so that the public localized read/write memory is addressable by the host processor. Robinson-2 teaches at least one class processor further comprises a public localized read/write memory and the class processor having the public localized read/write memory is configured so that the public localized read/write memory is addressable by the host processor (The system object ... common to all objects; col. 9, lines 32-39 and the host may send global configurations to the system object ... instantiate this particular object; col. 12, lines 29-49).

16. **As to claim 11**, Robinson-1 does not teach the class processors are controlled and activated by the host processor. Robinson-2 teaches the class processors are controlled and activated by the host processor (In response to a high level command form a host processor ... to instantiate itself in RAM; col. 5, lines 6-9).

17. **As to claim 12**, Robinson-1 does not teach the class processors are controlled and activated by the host processor exclusively via the application program interface modules. Robinson-2 teaches the class processors are controlled and activated by the host processor exclusively via the application program interface modules (In response to a high level command form a host processor ... to instantiate itself in RAM; col. 5, lines 6-9).

18. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Robinson (U.S. 5,708,838, now refer as Robinson-1) in view of Robinson (U.S. 6,567,837 B1, now refer as Robinson-2) further in view of Kneib (U.S. 4,641,238).

19. **As to claim 6**, Robinson-1 does not teach semi-private busses coupled to the class processors of the same class providing access to the protected localized read/write memory. Kneib teaches a semi-private bus coupled to the class processors for communication between class processors (Serial bus 20; col. 4, lines 35-40 and Fig. 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Robinson-1, Robinson-2 and Kneib because it allows to communication between each class processor independent of the bus used to communicate with the host processor (col. 7, lines 41-44).

20. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Robinson (U.S. 5,708,838, now refer as Robinson-1) in view of Patel et al. (U.S. 5,513,369).

21. **As to claim 13**, Robinson-1 teaches partitioning the application into functions and data messages (the code for the object oriented processors ... would be written as the main; col. 17, lines 62-67 and distributing processing tasks between a host processor and at least one object oriented processor; col. 4, lines 22-25), configuring a host processor having a host communication infrastructure to pass data messages via the HCI to control the application (the comms and interface routines; col. 12, line 66- col. 13, line 8), configuring a plurality of class processors to compute the functions into which the application is partitioned in response to the data messages (a plurality of object oriented processors 104, 106, 108; col. 7, lines 35-60 and each object oriented processor according to the invention is designed with a specific functionality; col. 14, lines 1-14), and interconnecting the class processors to the host processor via application program interface modules (Each of the object oriented processors includes a Comms interface ... to the host processor 102; col. 7, lines 35-60), the application program interface modules each defining a programming interface for a respective class processor (Each of the object oriented processors ...conventional manner; col. 7, lines41-49 and The comms and interface routines ... processor (the library provides the interface/API to be called while the implementation is inaccessible from uses); col. 13, lines 3-6 and the functionality of the pins ... the user interface 104; col. 14, lines 10-14).

22. However, Robinson-1 does not teach interconnecting the class processors to the host processor in a star configuration. Patel teaches interconnecting the class processors to the host processor in a star configuration (Each subsystem includes a plurality of processors 14 ... of each subsystem; col. 3, lines 15-18).

23. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Robinson-1 and Patel because it provides a new and useful method for interconnecting processors within a distributed data processing system (col. 2, lines 1-3).

24. Claims 14 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robinson (U.S. 5,708,838, now refer as Robinson-1) in view of Patel et al. (U.S. 5,513,369) further in view of Robinson (U.S. 6,567,837 B1, now refer as Robinson-2).

25. **As to claim 14**, Robinson-1 does not teach at least one class processor comprises a private localized read/write memory, and protecting the private localized read/write memory from being read and from being altered by the host processor and the other class processors, except in response to predefined data messages sent to an application program interface module instructing the class processor to execute a function. Robinson-2 teaches at least one class processor comprises a private localized read/write memory (one or more parts of Ram are arranged for private data; col. 10, lines 11-41), and protecting the private localized read/write memory from being read and from being altered by the host processor and the other class processors (One or more other parts of RAM are ... its functionality; col. 10, lines 11-41), except in response to predefined data messages sent to an application program interface module instructing the class processor to execute a function (One or more other parts of RAM are ... its functionality; col. 10, lines 11-41 and the input message ... for named instantiation of the object;

col. 5, lines 44-52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Robinson-1 and Robinson-2 because it provides an object oriented processor array that utilizes memory in an efficient manner (col. 4, lines 23-25).

26. **As to claim 17**, Robinson-1 does not explicitly teach wherein partitioning the application into functions and data messages comprises the steps of identifying signals as objects and transforms of signals as functions, grouping functions into groups of related functions independent of others of the groups of related functions, and configuring each of the plurality of class processors to compute a group of related functions to reduce communication between class processors and the host processor. Robinson-1 teaches an object oriented processor with speech processing functionality, wherein the functionality layer is implemented by the analog and digital converter, and the analog audio signals is converted into digital signals (col. 16, lines 1-36), Robinson-1 further teaches the code for each object oriented processor would be written as class (col. 17, lines 62-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to improve the system of Robinson-1 because in object oriented programming language, noun could be implemented as object and verb could be implemented as function.

27. **As to claim 18**, Robinson-1 does not explicitly teach grouping functions into groups of related functions that have independent data structures, and configuring each of the plurality of data structures comprises configuring each of the class processors to have no knowledge of data

structures in other class processors and to communicate with other class processors only through their respective application programming interface modules. However, Robinson-1 teaches the code for each object-oriented processor would be written as class (col. 17, lines 62-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made the system of Robinson-1 would have implemented the above because it bases on the fundamental of object oriented programming language.

28. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robinson (U.S. 5,708,838, now refer as Robinson-1) in view of Robinson (U.S. 6,567,837 B1, now refer as Robinson-2) and Patel et al. (U.S. 5,513,369) further in view of Admitted Prior Art (APA).

29. **As to claim 15**, Robinson-1 does not teach forming the distributed processing system on an integrated circuit chip, and locating class processors for executing functions most frequently required by the application most physically proximate the host processor on the integrated circuit chip. APA teaches the distributed processing system is integrated onto a single chip substrate (on the chip; page 1, lines 15-27), and interconnecting the processors via at least one member of the group of interconnections consisting of virtual socket interfaces, communication backbones, interface buses (page 1, lines 20-26). It would have been obvious to apply the teaching of APA to the system of Robinson-1 because it provides powerful computational platforms on a single chip, and since the processors are connected via buses, it would have been obvious to put the processor that is most frequently required by the host closes to the host because it provides less

time for communication.

**30.** **As to claim 16**, Robinson-1 teaches the code for each object oriented processor would be written as class (col. 17, lines 62-67), each object oriented processor according to the invention is designed with a specific functionality (col. 14, lines 1-14), and two or more object oriented processors having the same type of task (col. 8, lines 35-38). However, Robinson-1 does not teach grouping functions into groups of related functions, interconnecting a group of class processors for executing a group of related functions, the group of class processors including the class processor having the protected read/write memory so that the protected read/write memory is accessible to a plurality of the group of class processors, and protecting the protected read/write memory from being read and from being altered by the host processor and other class processors not in the group of class processors. Robinson-2 teaches at least one of the class processors has an associated protected localized read/write memory accessible only to itself and to at least one other class processor of the same class (When an object is instantiated ... their allocated RAM in this manner; col. 10, lines 30-35 and the microprocessors 523a-c provide separate processors for each instantiation of an object ... loading software into one of the processors 523a-c; col. 17, line 63 - col. 18, line 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Robinson-1 and Robinson-2 because it provides an object oriented processor array with enhanced post-manufacture configurability.

31. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Robinson (U.S.

5,708,838, now refer as Robinson-1) in view of Patel et al. (U.S. 5,513,369) further in view of Admitted Prior Art (APA).

32. **As to claim 19**, Robinson-1 as modified does not teach wherein interconnecting the class processors to the host processor via application program interface modules in a star configuration comprises the step of interconnecting the class processors to the host processor via at least one member of the group of interconnections consisting of virtual socket interfaces, I/O port data exchange interfaces, memory mapped dual port random access memory banks, stacks, and first-in-first-out memory. APA teaches the step of interconnecting the processors via at least one member of the group of interconnections consisting of virtual socket interfaces, communication backbones, and interface buses (page 1, lines 20-26). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Robinson-1 and APA because it provides a unified environment.

### *Response to Arguments*

33. Applicant's arguments filed 10/29/2004 have been fully considered but they are not persuasive. Please refer to the rejection above and the last Office action for Examiner position.

### *Conclusion*

34. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Dangelo (U.S. 5,946,487) teaches Object-oriented multi-media architecture.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Diem K Cao whose telephone number is (571) 272-3760. The examiner can normally be reached on Monday - Friday, 8:00AM - 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**Any response to this action should be mailed to:**
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist at 571-272-2100.

Due to the realignment of WG 2120, effective March 20, 2005, AU 2126 will become AU 2194.

Diem Cao

MENG-AL T. AN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100